

Fabrication-constrained inverse design of a broadband 3-way power splitter

Alexander Y. Piggott,¹ Jan Petykiewicz,¹ Logan Su,¹ and Jelena Vučković¹

¹*Ginzton Laboratory, Stanford University, Stanford, California 94305, USA*

(Dated: December 15, 2016)

A major difficulty in applying computational design methods to nanophotonic devices is ensuring that the resulting designs are fabricable. Here, we describe a general inverse design algorithm for nanophotonic devices that directly incorporates fabrication constraints. To demonstrate the capabilities of our method, we designed and experimentally demonstrated a compact, broadband 1×3 power splitter on a silicon photonics platform. The splitter has a footprint of only $3.8 \times 2.5 \mu\text{m}$, and is well within the design rules of a typical silicon photonics process, with a minimum radius of curvature of 100 nm. Averaged over the designed wavelength range of 1400 – 1700 nm, our device has a measured insertion loss of 0.642 ± 0.057 dB and power uniformity of 0.641 ± 0.054 dB.

I. INTRODUCTION

Nanophotonic devices are typically designed by starting with an analytically designed structure, and hand-tuning a few parameters [1]. In recent years, it has become increasingly popular to automate this process with the use of powerful optimization algorithms. In particular, by searching the full space of possible structures, it is possible to design devices with higher performance and smaller footprints than traditional devices [2–8].

A major challenge when designing devices with arbitrary topologies is ensuring that the structures remain fabricable. Many of these computationally designed structures have excellent performance when fabricated using high-resolution electron-beam lithography, but they have features which are difficult to resolve with industry-standard optical lithography [3, 7, 8].

Meanwhile, robust and efficient power splitters are essential building blocks for integrated photonics. A variety of 1×2 splitters with attractive performance have been demonstrated on the silicon photonics platform, ranging from conventional devices [9, 10] to those designed using advanced optimization techniques [4, 11, 12]. However, it is not possible to split power equally into an arbitrary number of waveguides by cascading 1×2 splitters, and efficient devices that fill this gap are lacking in the literature.

Building on our previous work [5, 7, 13], we propose an inverse design method for nanophotonic devices that incorporates fabrication constraints. Our algorithm achieves an approximate minimum feature size by imposing curvature constraints on dielectric boundaries in the structure. We then demonstrate the capabilities of our method by designing and experimentally demonstrating a broadband 1×3 power splitter. The splitter has no small features, and should be fabricable by any modern CMOS photonics process.

II. DESIGN METHOD

Due to the complexity of accurately modelling lithography and etching processes, most attempts to incorpo-

rate fabrication constraints into computational nanophotonic design have focused on heuristic methods. One approach is to restrict the design to rectangular pixels which are larger than the minimum allowable feature size [14]. The resulting Manhattan geometry, however, is restrictive and likely not optimal for optical devices. Another method involves applying a convolutional filter to the design followed by thresholding [15–17], which can introduce artifacts smaller than the desired feature size. The approach used in this work is to impose curvature constraints on the device boundaries, which avoids the aforementioned issues. Curvature limits have been successfully applied in earlier work [4], but were not described in detail nor validated with experimental demonstrations.

A. Level Set Formulation

We assume that our device is planar and consists of only two materials. We can represent our structure by constructing a continuous function $\phi(x, y) : \mathbb{R}^2 \rightarrow \mathbb{R}$ over our design region, and letting the boundaries between the materials lie on the level set $\phi = 0$. The permittivity ϵ is then given by

$$\epsilon(x, y) = \begin{cases} \epsilon_1 & \text{for } \phi(x, y) \leq 0 \\ \epsilon_2 & \text{for } \phi(x, y) > 0. \end{cases} \quad (1)$$

The advantage of this implicit representation is that changes in topology, such as the merging and splitting of holes, are trivial to handle. We can also manipulate our structure by adding a time dependence, and evolving $\phi(x, y, t)$ as a function of time t with a variety of partial differential equations collectively known as level set methods [18, 19].

To design a device, we first choose some objective function $f[\epsilon]$ which describes how well the structure matches our electromagnetic performance constraints [5, 7]. We then evolve our structure, represented by ϕ , in such a way that we minimize our objective f . We can achieve this by adapting gradient descent optimization to our level set representation. The level set equation for moving

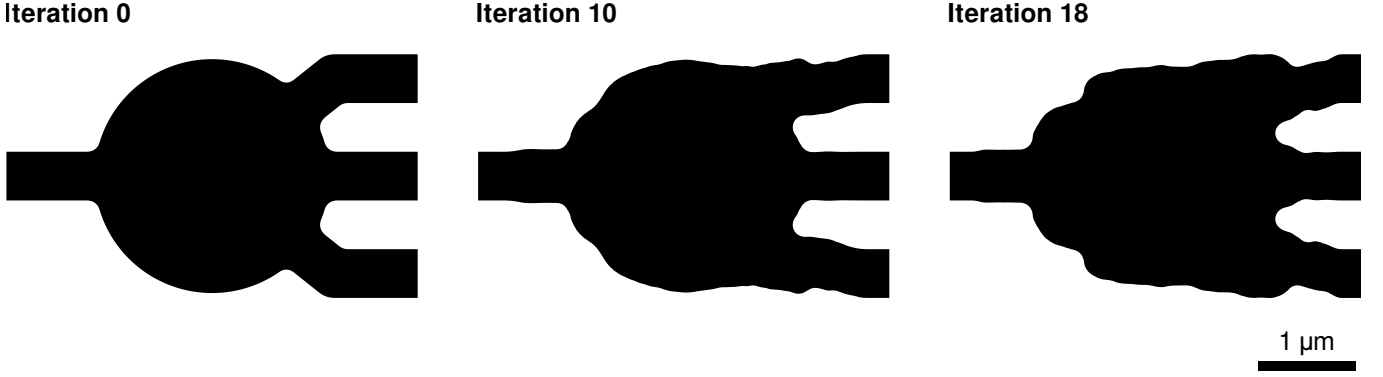


FIG. 1: Intermediate steps in the optimization process for the 1×3 splitter. Starting with a star-shaped geometry, the optimization converged in 18 iterations. The minimum radius of curvature in the design was set to 100 nm. Regions with Si are denoted in black, and SiO_2 is denoted in white.

boundaries in the normal direction is

$$\phi_t + v(x, y) |\nabla \phi| = 0 \quad (2)$$

where $\nabla \phi = \phi_x + \phi_y$ is the spatial gradient of ϕ , and $v(x, y)$ is the local velocity. To implement gradient descent, we choose the velocity field $v(x, y)$ to correspond to the gradient of the objective function $f[\epsilon]$ [19], which can be efficiently computed using adjoint sensitivity analysis [3, 4, 6, 13]. As $t \rightarrow \infty$, ϕ converges to a locally optimal structure.

Unfortunately, this approach tends to result in the formation of extremely small features. We can avoid this problem by periodically enforcing curvature constraints. The level set equation for smoothing out curved regions is

$$\phi_t - \kappa |\nabla \phi| = 0 \quad (3)$$

where the local curvature κ is given by

$$\kappa = \nabla \cdot \left(\frac{\nabla \phi}{|\nabla \phi|} \right) = \frac{\phi_x^2 \phi_{yy} - 2\phi_x \phi_y \phi_{xy} + \phi_{xx} \phi_y^2}{|\nabla \phi|^3}. \quad (4)$$

Although equation 3 removes highly curved regions more quickly [18], the boundaries are eventually reduced to a set of straight lines with zero curvature as $t \rightarrow \infty$.

From a fabrication perspective, we only need to smooth regions which are above some maximum allowable curvature κ_0 . We can do this by introducing a weighting function

$$b(\kappa) = \begin{cases} 1 & \text{for } |\kappa| > \kappa_0 \\ 0 & \text{otherwise} \end{cases} \quad (5)$$

and modifying equation 3 to be

$$\phi_t - b(\kappa) \kappa |\nabla \phi| = 0. \quad (6)$$

If we evolve ϕ with equation 6 until it reaches steady state, the maximum curvature will be less than or equal to κ_0 .

The final design algorithm is as follows:

1. Initialize ϕ and δt .
2. Repeat until $\delta t < \delta t_{min}$.
 - (a) Let $\phi' \leftarrow \phi$.
 - (b) **Gradient descent**: evolve ϕ' with eqn. 2 for time δt .
 - (c) **Curvature limit**: evolve ϕ' with eqn. 6 until convergence.
 - (d) **If** $f[\epsilon[\phi']] < f[\epsilon[\phi]]$, **then** let $\phi \leftarrow \phi'$ and increase δt .
Otherwise, decrease δt .

Implementation details can be found in the supplementary information.

B. Power splitter design

In designing the 1×3 power splitter, we chose the structure to consist of a single fully-etched 220 nm thick Si layer with SiO_2 cladding. Refractive indices of $n_{\text{Si}} = 3.48$ and $n_{\text{SiO}_2} = 1.44$ were used. The waveguide width was set to 500 nm for both the input and output waveguides. We constrained the minimum radius of curvature to be 100 nm, well within the typical design rules of a CMOS silicon photonics process. We also enforced bilateral symmetry for the structure.

The splitter was designed at 6 equally spaced wavelengths between 1400–1700 nm. We specified that power in the fundamental transverse-electric (TE) mode of the input waveguide should be equally split into the fundamental TE mode of the three output waveguides, with at least 95% efficiency.

The optimization process is illustrated in figure 1. Starting with a star-shaped geometry, the optimization process converged in 18 iterations. The device was designed in approximately 2 hours on a single server with an Intel Core i7-5820K processor, 64GB of RAM, and three Nvidia Titan Z graphics cards. All electromagnetic

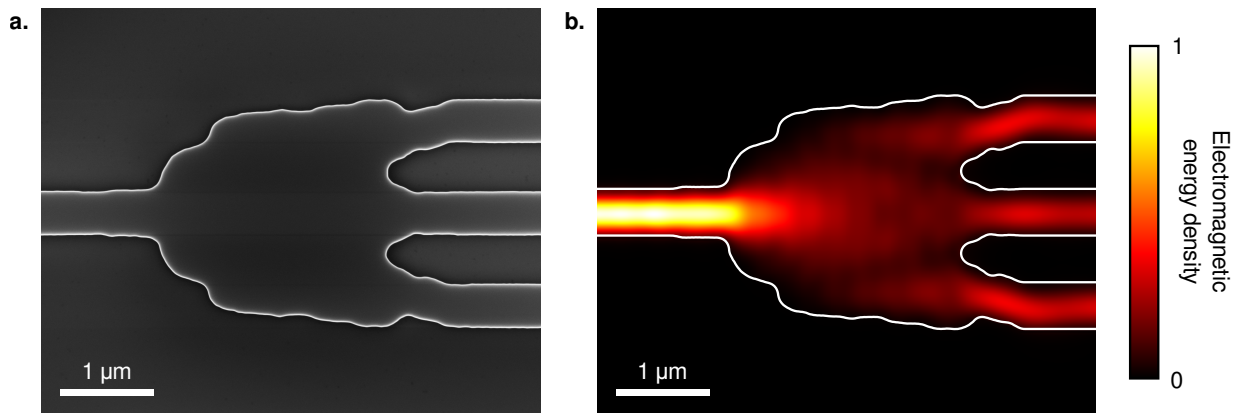


FIG. 2: The broadband 1×3 splitter. **(a)** SEM image of the fabricated splitter. The device was made by fully etching the 220 nm device layer of an SOI wafer. The total footprint is $3.8 \times 2.5 \mu\text{m}$. This image was taken before the devices were capped with oxide. **(b)** Electromagnetic energy density in the device at 1550 nm. The fields were calculated using finite-difference time-domain (FDTD) simulations. The boundaries of the device are outlined in white.

simulations were performed using a graphical processing unit (GPU) accelerated implementation of the finite-difference frequency-domain (FDFD) method [20, 21].

III. EXPERIMENTAL RESULTS

A. Fabrication

The power splitters were fabricated on Unibond Smart-Cut silicon-on-insulator (SOI) wafers obtained from SOITEC, with a nominal 220 nm device layer, and $3.0 \mu\text{m}$ buried oxide layer. A JEOL JBX-6300FS electron-beam lithography system was used to pattern a 330 nm thick layer of ZEP-520A resist spun on the samples. A transformer-coupled plasma etcher was used to transfer the pattern to the device layer, using a C_2F_6 break-through step and $\text{BCl}_3/\text{Cl}_2/\text{O}_2$ main etch. The mask was stripped by soaking in solvents, followed by a piranha ($\text{H}_2\text{SO}_4/\text{H}_2\text{O}_2$) clean. Finally, the devices were capped with $1.6 \mu\text{m}$ of LPCVD (low pressure chemical vapour deposition) oxide.

A multi-step etch-based process was used to expose waveguide facets for edge coupling. First, a chrome mask was deposited using liftoff to protect the devices. Next, the oxide cladding, device layer, and buried oxide layer were etched in an inductively-coupled plasma etcher using a $\text{C}_4\text{F}_8/\text{ArO}_2$ chemistry. To provide mechanical clearance for the optical fibers, the silicon substrate was then etched to a depth of $\sim 100 \mu\text{m}$ using the Bosch process in a deep reactive-ion etcher (DRIE). Finally, the chrome mask was chemically stripped, and the samples were diced into conveniently-sized pieces.

B. Characterization

The final splitter is illustrated in figure 2, showing both an scanning-electron micrograph (SEM) of the fabricated device, and simulated electromagnetic fields at the center wavelength of 1550 nm.

Transmission through the device was measured by edge-coupling to the input and output waveguides using lensed fibers. A polarization-maintaining fiber was used on the input side to ensure that only the TE mode of the waveguide was excited. To obtain consistent coupling regardless of the transmission spectra of the devices, the fibers were aligned by optimizing the transmitted power of a 1570 nm laser. The transmission spectrum was then measured by using a supercontinuum source and a spectrum analyzer. The device characteristics were obtained by normalizing the transmission with respect to a waveguide running parallel to the device.

The simulated and measured transmission spectra of the device are plotted in figure 3. The simulations and measurements match reasonably well, although the measured devices have slightly higher losses and exhibit a spectral shift with respect to simulations. The device performance is highly consistent across all 4 measured devices, indicating that they are robust to fabrication error.

The two key criteria for a power splitter are low insertion loss, and excellent power uniformity. The power uniformity is defined as the ratio between the maximum and minimum output powers. Averaged over the designed wavelength range of 1400 – 1700 nm, our 1×3 splitter has a measured insertion loss of 0.642 ± 0.057 dB, and a power uniformity of 0.641 ± 0.054 dB. Here, the uncertainty refers to the variability between different measured devices.

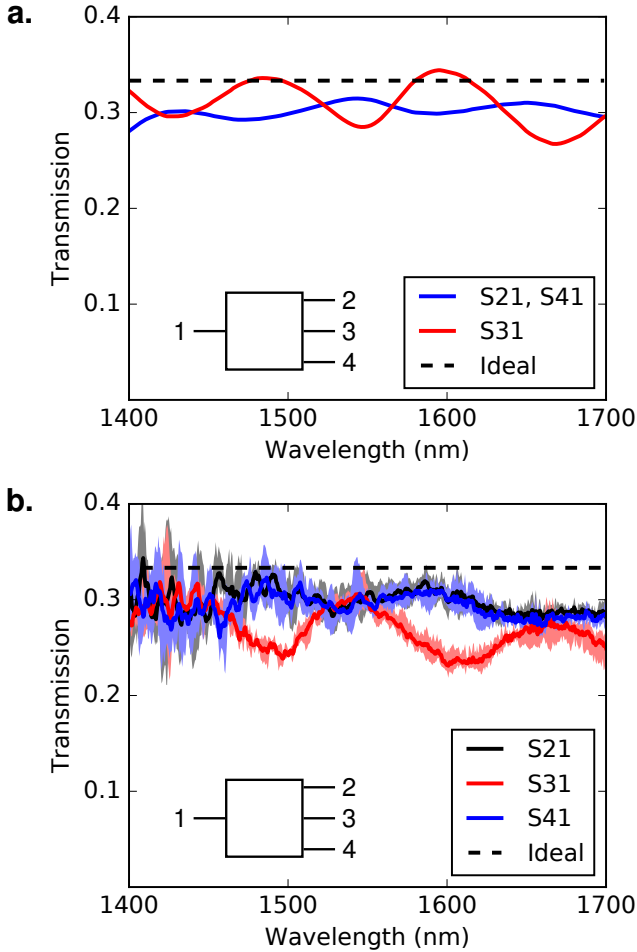


FIG. 3: Simulated and measured S-parameters for the broadband 1×3 splitter, where S_{ij} is the transmission from port i to port j . **(a)** Simulated performance, calculated using finite-difference time-domain (FDTD) simulations. Due to bilateral symmetry in the structure, S_{21} and S_{41} are equal to each other. **(b)** Measured device performance. Here, we have overlaid the measurements for 4 identically fabricated devices. The average values are denoted by the solid lines, and the minimum and maximum values are denoted by the shaded areas.

IV. CONCLUSION

In summary, we have incorporated fabrication constraints into an inverse design algorithm for nanophotonic devices. Using this method, we designed and experimentally demonstrated a broadband 1×3 splitter. Critically, the device has no small features which would violate the design rules of a standard silicon photonics process, paving the way for inverse designed structures to become practical components of integrated photonics systems.

Acknowledgments

This work was funded by the AFOSR MURI for Aperiodic Silicon Photonics, grant number FA9550-15-1-0335, the Gordon and Betty Moore Foundation, and Global-Foundries Inc. All devices were fabricated at the Stanford Nanofabrication Facility (SNF) and Stanford Nano Shared Facilities (SNSF).

-
- [1] G. T. Reed, *Silicon Photonics: The State of the Art* (John Wiley & Sons, Chichester, West Sussex, U.K., 2008).
 - [2] A. Mutapcica, S. Boyd, A. Farjadpour, S. G. Johnson, and Y. Avnielb, “Robust design of slow-light tapers in periodic waveguides,” *Eng. Optimiz.* **41**, 365 – 384 (2009).
 - [3] J. S. Jensen and O. Sigmund, “Topology optimization for nano-photonics,” *Laser Photonics Rev.* **5**, 308 – 321 (2011).
 - [4] C. M. Lalau-Keraly, S. Bhargava, O. D. Miller, and E. Yablonovitch, “Adjoint shape optimization applied to electromagnetic design,” *Opt. Express* **21**, 21693 – 21701 (2013).
 - [5] J. Lu and J. Vučković, “Nanophotonic computational design,” *Opt. Express* **21**, 13351 – 13367 (2013).
 - [6] A. C. R. Niederberger, D. A. Fattal, N. R. Gauger, S. Fan, and R. G. Beausoleil, “Sensitivity analysis and optimization of sub-wavelength optical gratings using adjoints,” *Opt. Express* **22**, 12971 – 12981 (2014).
 - [7] A. Y. Piggott, J. Lu, K. G. Lagoudakis, J. Petykiewicz, T. M. Babinec, and J. Vučković, “Inverse design and demonstration of a compact and broadband on-chip wavelength demultiplexer,” *Nature Photonics* **9**, 374–377 (2015).
 - [8] L. F. Frellsen, Y. Ding, O. Sigmund, and L. H. Frandsen, “Topology optimized mode multiplexing in silicon-on-insulator photonic wire waveguides,” *Opt. Express* **24**,

- 16866 – 16873 (2016).
- [9] A. Sakai, T. Fukuzawa, and T. Baba, “Low loss ultra-small branches in a silicon photonic wire waveguide,” *IEICE Trans. Electron.* **E85-C**, 1033 – 1038 (2002).
 - [10] S. H. Tao, Q. Fang, J. F. Song, M. B. Yu, G. Q. Lo, and D. L. Kwong, “Cascade wide-angle y-junction 1×16 optical power splitter based on silicon wire waveguides on silicon-on-insulator,” *Opt. Express* **16**, 21456–21461 (2008).
 - [11] P. I. Borel, L. H. Frandsen, A. Harpøth, M. Kristensen, J. S. Jensen, and O. Sigmund, “Topology optimised broadband photonic crystal y-splitter,” *Electron. Lett.* **41**, 69–71 (2005).
 - [12] Y. Zhang, S. Yang, A. E.-J. Lim, G.-Q. Lo, C. Galland, T. Baehr-Jones, and M. Hochberg, “A compact and low loss y-junction for submicron silicon waveguide,” *Opt. Express* **21**, 1310–1316 (2013).
 - [13] A. Y. Piggott, J. Lu, T. M. Babinec, K. G. Lagoudakis, J. Petykiewicz, and J. Vučković, “Inverse design and implementation of a wavelength demultiplexing grating coupler,” *Sci. Rep.* **4**, 7210 (2014).
 - [14] B. Shen, P. Wang, R. Polson, and R. Menon, “An integrated-nanophotonics polarization beamsplitter with $2.4 \times 2.4 \mu\text{m}$ footprint,” *Nature Photonics* **9**, 378 – 382 (2015).
 - [15] Y. Elesin, B. Lazarov, J. Jensen, and O. Sigmund, “Design of robust and efficient photonic switches using topology optimization,” *Phot. Nano. Fund. Appl.* **10**, 153 – 165 (2012).
 - [16] Y. Deng and J. G. Korvink, “Topology optimization for three-dimensional electromagnetic waves using an edge element-based finite-element method,” *Proc. R. Soc. A* **472**, 20150835 (2016).
 - [17] L. H. Frandsen and O. Sigmund, “Inverse design engineering of all-silicon polarization beam splitters,” *Proc. SPIE* **9756**, 97560Y–1 – 97560Y–6 (2016).
 - [18] S. Osher and R. Fedkiw, *Level Set Methods and Dynamic Implicit Surfaces* (Springer, New York, U.S.A., 2003).
 - [19] M. Burger and S. J. Osher, “A survey on level set methods for inverse problems and optimal design,” *Eur. J. Appl. Math.* **16**, 263 – 301 (2005).
 - [20] W. Shin and S. Fan, “Choice of the perfectly matched layer boundary condition for frequency-domain Maxwell’s equations solvers,” *J. Comput. Phys.* **231**, 3406 – 3431 (2012).
 - [21] W. Shin and S. Fan, “Accelerated solution of the frequency-domain Maxwell’s equations by engineering the eigenvalue distribution,” *Opt. Express* **21**, 22578 – 22595 (2013).

Supplemental Information

V. LEVEL SET IMPLEMENTATION

A. Curvature limiting

In the main text, we wrote that we implement curvature limiting by evolving the level set function ϕ with

$$\phi_t - b(\kappa)\kappa |\nabla \phi| = 0 \quad (\text{S1})$$

using the weighting function

$$b(\kappa) = \begin{cases} 1 & \text{for } |\kappa| > \kappa_0 \\ 0 & \text{otherwise.} \end{cases} \quad (\text{S2})$$

In practice, this has terrible convergence since the weighting function falls off infinitely sharply as the local curvature crosses κ_0 . To improve the behaviour of our PDE, we actually use a smoothed weighting function

$$b(x, y) = \exp(-\kappa_0^2 d^2(x, y)), \quad (\text{S3})$$

where $d(x, y)$ is the Euclidean distance to the nearest element in the set $\Omega = \{(x, y) | \kappa(x, y) > \kappa_0\}$,

$$d(x, y) = \inf_{(\hat{x}, \hat{y}) \in \Omega} \|(x, y) - (\hat{x}, \hat{y})\|. \quad (\text{S4})$$

The distance function $d(x, y)$ can be efficiently computed using the Euclidean distance transform commonly included in image processing libraries.

B. Numerical implementation

In our design algorithm, we apply gradient descent with the partial differential equation

$$\phi_t + v(x, y) |\nabla \phi| = 0 \quad (\text{S5})$$

where $v(x, y)$ is the local velocity, and apply curvature limiting with equation S1. We spatially discretize equation S5 using Godunov's scheme, and equation S1 using central differencing, as is common practice [S1]. We discretize in the time dimension using Euler's method.

To ensure that our level set equations remain well behaved, we regularly reinitialize ϕ to be a signed distance function [S1], where $|\nabla \phi| \approx 1$. Most reinitialization schemes, however, result in subtle shifts in the interface locations, which can cause optimization to fail. We use Russo and Smerka's reinitialization scheme to avoid these issues [S2].

[S1] S. Osher and R. Fedkiw, *Level Set Methods and Dynamic Implicit Surfaces* (Springer, New York, U.S.A., 2003).

[S2] G. Russo and P. Smereka, "A remark on computing dis-

tance functions," J. Comput. Phys. **163**, 51 – 67 (2000).